# Gigabit Serial Link Controller IP Core

Space applications require more and more high speed serial links to sustain the ever increasing data-rate demands of satellites while keeping the harness routing complexity under control.

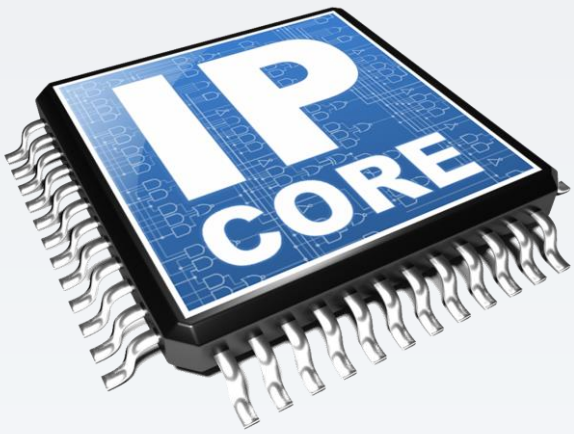
The Gigabit Serial Link Controller (GSLC) IP core implements the digital interface for both simple and complex communication protocols based on the most used Serializer/Deserializer (SERDES) available on the market.

The GSLC can be customised to be compatible with a very simple hand-shake/flow control protocol or with a more complex communication standard including FDIR and Quality-of-Service such as SpaceFibre.

The GSLC IP is suitable both for FPGA and ASIC technology depending on the application demand.

## Key Features

- Customisable to fulfil user needs
- 6.6 Gbps link speed on the Xilinx Virtex-6 GTX transceiver
- Compatible with Microsemi RTAX2000 FPGA + Wizard Link TLK2711 configuration
- Compliant with the SpaceFibre standard
- Interoperable with commercial SpaceFibre products
- Available with simple FIFO-based host interface or AXI-based DMA interface (other host interfacing options are available on request)
- Compliant with the most common SERDES units (WizardLink, RocketIO, GTX)
- Compliance with other SERDES available on request



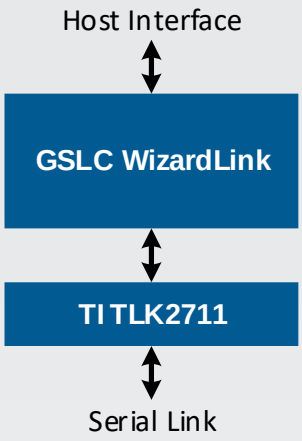

INGENIArs

IngeniArs SpaceFibre technologies have been developed in the framework of the project SIMPLE (Spacefibre IMPLementation design & test Equipment). This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 757038.

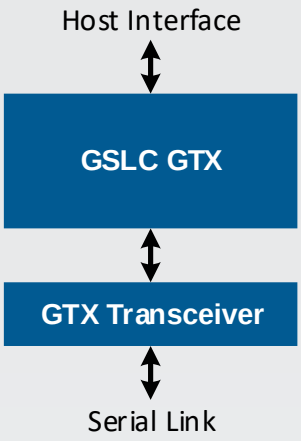
# Typical scenarios

The Gigabit Serial Link Controller is a highly customisable block which can be used in different scenarios:

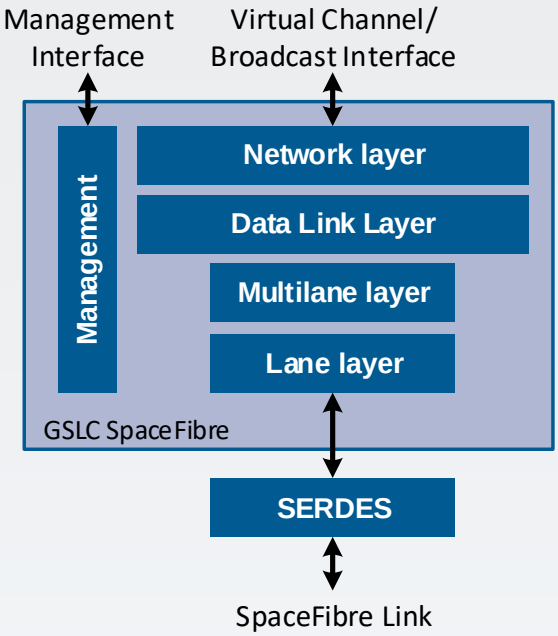
## Interface for Texas Instruments TLK2711 (WizardLink)




## Interface for Xilinx transceivers (RocketIO, GTX, …)




## SpaceFibre interface




## Customisable on user request

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# Synthesis results on Microsemi RTAX2000S FPGA

| | Combinational | Registers | RAM blocks |
|---|---|---|---|
| GSLC Wizardlink | 3.3 % (713/21504) | 3.1 % (335/10752) | 6.3 % (4/64) |
| GSLC SpaceFibre (2 VCs) | 22 % (4641/21504) | 14 % (1471/10752) | 19 % (12/64) |
| GSLC SpaceFibre (4 VCs) | 29 % (6201/21504) | 19 % (2091/10572) | 25 % (16/64) |


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