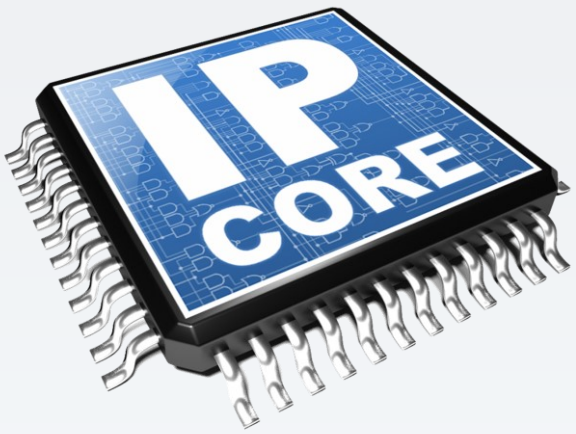
SpaceWire Router IP Core

The SpaceWire Router IP core is a macrocell offering a configurable and flexible solution for high data-rate routing switch functionality for on-board satellite networking. It is based on the SpaceWire protocol, defining bi-directional, full-duplex, serial data communication link, and it is compliant with the SpaceWire standard ECSS-E-ST-50-12C.

The SpaceWire Router IP Core features a parameterised number of SpaceWire ports, based on the SpaceWire CODEC IP Core, and host-side data ports, based on simple asynchronous FIFO interfaces. The host data ports can be equipped (on request) with AMBA AXI interface. The SpaceWire Router IP core has been validated and prototyped in ESA project.

Key Features

- ECSS-E-ST-50-12C compliant (routing switch specification)
- Highly customisable to fulfil user needs
- Up to 31 SpaceWire and/or host data ports
- Path addressing, logical addressing and regional addressing support
- SpaceWire TX data-rate and link start mode programmability for each available SpaceWire port
- Host data ports with simple FIFO-based interface or optional AMBA AXI bus interface (on request)
- Time-code distribution support
- SpaceWire links configuration/check and addresses mapping via SpaceWire packets
- Optional support to RMAP commands (under development)
- SpaceWire links configuration/check also possible through dedicated host port
- Synthesized on rad-tolerant FPGA and other devices



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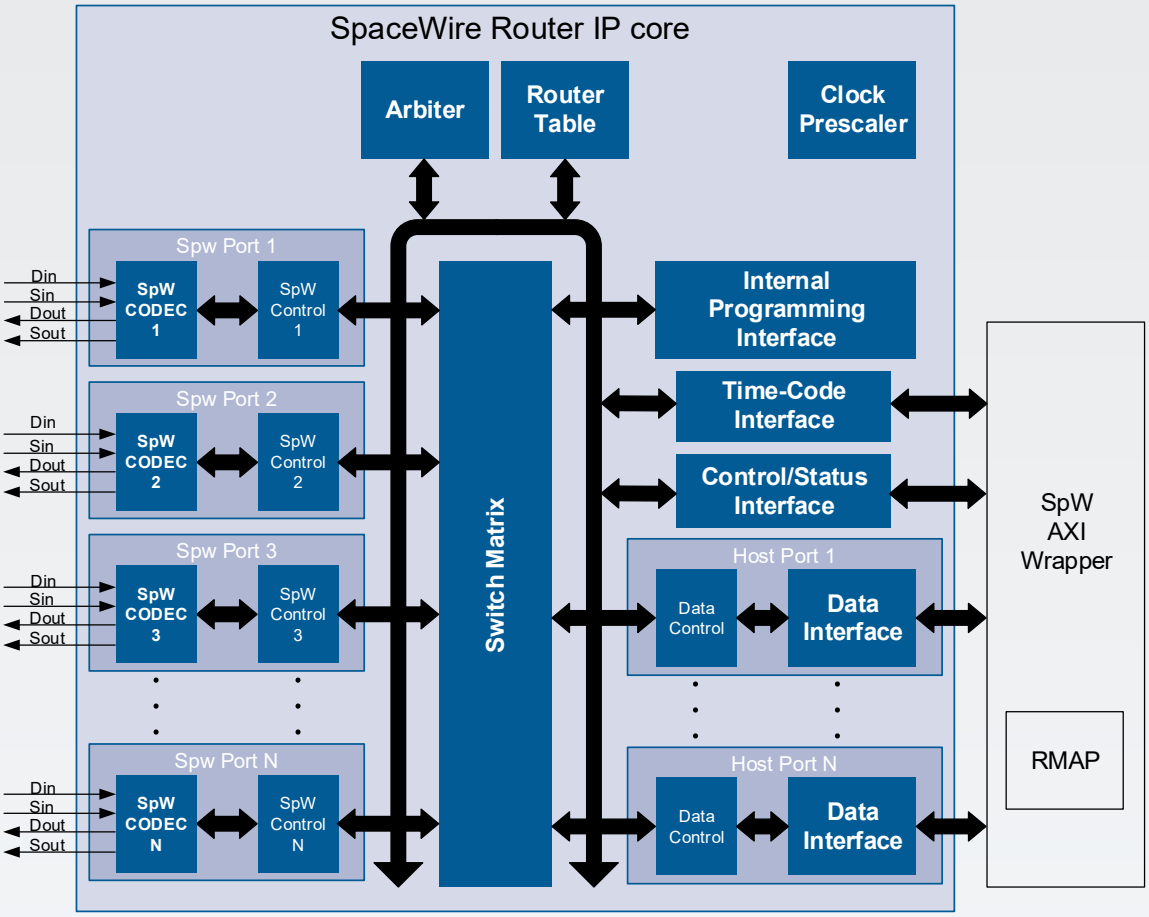
Architectural features

Besides the parameterised number of SpaceWire ports and host data ports, the architecture features the following units: switch matrix, fully programmable router table, arbiter logic, programming interface, time-code host interface, and control/status host interface.

The SpaceWire port units and the host data port units offer data connectivity between nodes. In particular, the host data ports can be equipped (on request) with AMBA AXI interface. The switch matrix, with router table and arbiter, dynamically connect the input nodes with the appropriate output nodes, relying on packet addressing. The programming interface allows SpaceWire links configuration/check and logical/regional addresses mapping. The control/status interface allows direct SpaceWire links configuration/check by the host system. RMAP commands also can be supported using a specific hardware decoder (under development). The time-code interface offers support to time-codes distribution throughout the network: the time-codes received by the router on any port are checked and forwarded to all the other network nodes.



Synthesis results on Microsemi RTAX2000S FPGA

	Combinational	Registers	RAM blocks
4 SpW ports + 1 host port	30.576% (6575/21504)	40.718% (4378/10752)	15.625 % (10/64)
8 SpW ports + 1 host port	52.097% (11203/21504)	63.402% (6817/10752)	28.125 % (18/64)

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