

CCSDS 131.2-B Receiver IP Core

The CCSDS 131.2-B Receiver IP Core is a complete solution to implement the core functions of a receiver compliant with the **CCSDS 131.2-B standard**: this standard has been conceived for Low Earth Observation mission with high data rate (more than 2 Gbps) and its primary application is to provide a complete solution for the implementation of a low-cost receiver based on commercial FPGAs to be used into the Ground Stations (Downlink application).

The main functions covered by the IP Core include the signal processing of the I/Q digital baseband signal, carrier frequency and phase recovery, timing recovery, demodulation of all the 27 Modulation and Coding formats (ModCodS) from QPSK to 8PSK and 16-, 32- and 64-APSK, and decoding based on Serially Concatenated Convolutional Codes (SCCC). In addition, the IP Core is suitable for integration into space qualified FPGA for the implementation of Uplink/Forward links application.

The CCSDS 131.2-B Receiver IP Core has been **developed within the framework of an ESA project.**

KEY FEATURES

- **Fully compliant with CCSDS 131.2-B standard**
- **Ground (Downlink) target applications:**
all the 27 ModCodS in a single instantiation based on commercial FPGAs (e.g., Intel Stratix 10, Xilinx Zynq/Virtex UltraScale+)
- **Space (Uplink) target applications:**
optimized configuration targeting FPGAs for space (e.g., Microchip PolarFire RT, Xilinx Kintex Ultrascale XQRKU060)
- **Baseband I/Q signal as input:**
frequency, phase and timing recovery loops
- **Carrier acquisition and tracking with Doppler effect up to 6.5 kHz/s of Doppler rate**
- **Dynamically configurable baud rate up to 500 MBaud**
- **Implementation loss lower than 2 dB with respect to performances reported in CCSDS 130.1-G-1 at CER 10^{-4} for ModCodS based on 64-APSK with AWGN, Doppler and phase noise**
- **Standard interfaces for easy integration based on AXI Lite and AXI Stream standards**
- **Optional mitigation techniques to safely operate in space environment:**
EDAC on internal memories, dead-lock free FSM design with one-hot encoding
- **Coded in technology-independent highly configurable VHDL**
- **Validation on commercial Xilinx VCU118 development kit for Downlink**